

What is claimed is:

1. A method for manufacturing a non-volatile memory device, comprising the steps of:

5 (a) forming an oxide layer on a substrate;

(b) implanting ions through the oxide layer to sequentially form a well in the substrate and a channel in the well;

(c) removing the oxide layer;

10 (d) depositing a tunnel oxide layer, a first polysilicon layer, and a nitride layer sequentially on the substrate;

15 (e) etching the nitride layer, the first polysilicon layer, the tunnel oxide layer and the substrate based on a shallow trench isolation pattern, resulting in a shallow trench in which the substrate is etched by a predetermined depth;

(f) filling the shallow trench with an isolation material;

20 (g) performing a polishing until the nitride layer is exposed to form a shallow trench isolation;

(h) removing the nitride layer to thereby protrude the shallow trench isolation; and

25 (i) depositing an oxide-nitride-oxide layer and a second polysilicon layer sequentially.

2. The method of claim 1, wherein the substrate is a silicon substrate.

3. The method of claim 1, wherein boron (B) and phosphor (P) are implanted for forming the well and the channel in the step (b).

4. The method of claim 1, wherein the oxide layer is removed by a wet etch in the step (c).

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5. The method of claim 1, wherein the polishing is performed by a chemical mechanical polishing in the step (g).

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6. The method of claim 1, wherein the nitride layer is removed by a wet etch in the step (h).